In the Claims:

1-51. (Canceled)

52. (New) A method of making a semiconductor memory device, the method comprising:

forming a plurality of trenches in a semiconductor body, the trenches being arranged in an array of rows and columns;

forming a dielectric material lining sidewalls of at least a lower portion of each trench;

filling at least the lower portion of each trench with a conductive material wherein the conductive material filling the trench forms a first plate of a capacitor and semiconductor material of the semiconductor body forms a second plate of the capacitor;

forming a trench collar lining a portion of a sidewall of each trench above the dielectric material;

forming a line mask over the semiconductor body after forming the plurality of trenches;

etching isolation trenches in alignment with a pattern of the line mask;

forming a plurality of isolation regions in the isolation trenches, each isolation region comprising a rectangular strip of insulating material that extends between adjacent columns of the trenches;

forming a plurality of pass transistors, each pass transistor having a first source/drain region and a second source/drain region, the first source/drain region being electrically coupled to the conductive material through an opening in the trench collar, the opening formed at one side of the trench such that an asymmetric trench structure is formed, each pair of a pass transistor and associated capacitor comprising a memory cell, wherein the second plate of the capacitor of each memory cell is coupled to the second plate of other memory cells;

forming a plurality of wordlines extending along the rows of the array of memory cells, each wordline being electrically coupled to a gate of every other memory cell along the row; and

forming a plurality of bitlines extending along the columns of the array of memory cells, each bitline being electrically coupled to the second source/drain region of every other memory cell along the column.

53. (New) The method of claim 52, wherein filling at least the lower portion of each trench comprises filling the lower portion of each trench with doped polysilicon.

54. (New) The method of claim 52, wherein adjacent ones of the trenches are separated by a distance of 3F, where F is a minimum feature size.

55. (New) The method of claim 52, wherein the first source/drain region of each pass transistor is vertically spaced from an upper surface of the semiconductor body such that each of the pass transistors comprises a vertical transistor.

56. (New) The method of claim 52, wherein a group of the trenches define a memory cell array and wherein the line mask includes equal lines and spaces that extend across an entire length of the memory cell array.

57. (New) The method of claim 52, wherein the line mask is formed after filling the lower portion of each trench with the conductive material.

58. (New) The method of claim 57, wherein the line mask includes equal lines.

59. (New) The method of claim 57, wherein the line mask is formed after forming the trench collar.

60. (New) The method of claim 52, wherein forming the trench collar comprises:

depositing a collar layer alongside walls of the trenches;

forming a pattern resist layer over the semiconductor body; and

etching back an exposed portion of the collar layer.

61. (New) A semiconductor memory device comprising:

an array of memory cells arranged in an array of rows and columns at a surface of a semiconductor body, each memory cell comprising:

a trench disposed within the semiconductor body;

a conductive material filling at least a lower portion of the trench;

a dielectric material lining sidewalls of the trench such that the conductive material filling the trench forms a first plate of a capacitor and semiconductor material of the semiconductor body forms a second plate of the capacitor, the second plate of the capacitor being electrically coupled to capacitors of other memory cells within the array;

a trench collar lining a portion of a sidewall of the trench above the dielectric material;

a pass transistor having a first source/drain region and a second source/drain region, the first source/drain region being electrically coupled to the conductive material through an opening in the trench collar, the opening formed at one side of the trench such that an asymmetric trench structure is formed;

a plurality of wordlines extending along the rows of the array of memory cells, each

wordline being electrically coupled to a gate of every other memory cell along the row;

a plurality of bitlines extending along the columns of the array of memory cells, each bitline being electrically coupled to the second source/drain region of every other memory cell along the column; and

a plurality of isolation regions extending parallel to the plurality of bitlines and disposed between columns of the array of memory cells, each isolation region comprising a rectangular strip of insulating material that extends between adjacent columns of the memory cells, wherein adjacent ones of the memory cells within a column are isolated without use of the isolation regions.

62. (New) The device of claim 61, wherein each isolation region has a width and is separated from a parallel isolation by a spacing distance, wherein the width is equal to the spacing distance.

63. (New) The device of claim 61, wherein adjacent ones of the trenches are separated by a distance 3F, where F is a minimum feature size.

64. (New) The device of claim 61, wherein each pass transistor comprises a vertical transistor.

65. (New) The device of claim 61, wherein, for each memory cell, the second source/drain region is located at the surface of the semiconductor body and the first source/drain region is located within the semiconductor body spaced from the surface.

66. (New) The device of claim 61, wherein the conductive material filling at least the lower portion of the trench comprises doped polysilicon.

67. (New) The device of claim 61, wherein the second plate of the capacitor comprises a doped region of the semiconductor body that extends beneath ones of the trenches.